Dual N-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

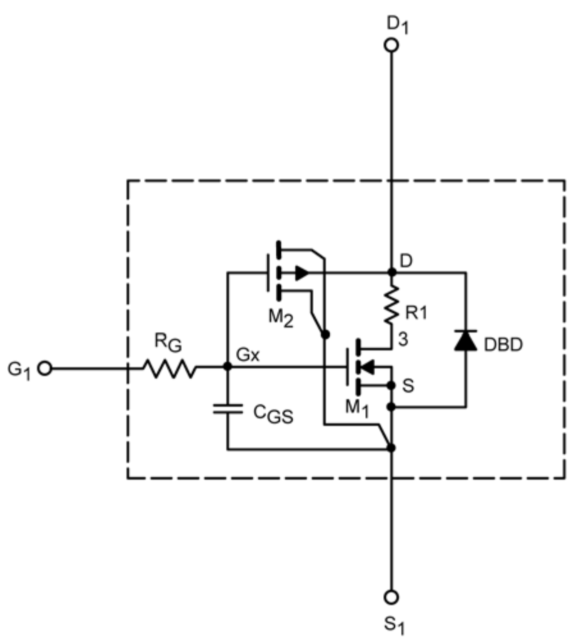
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

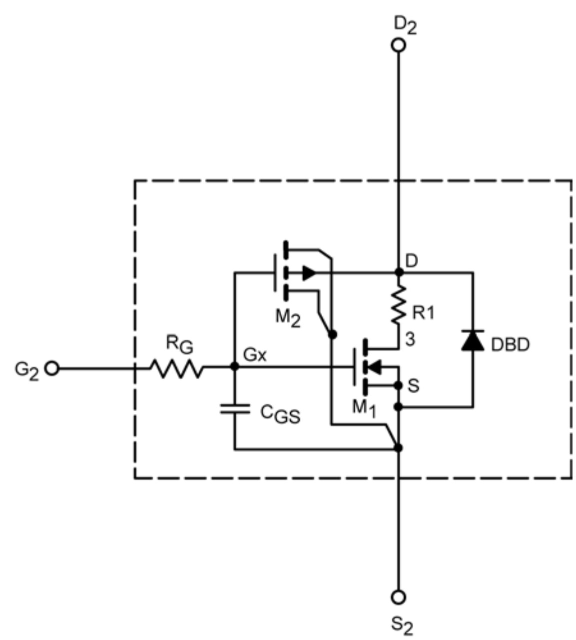
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





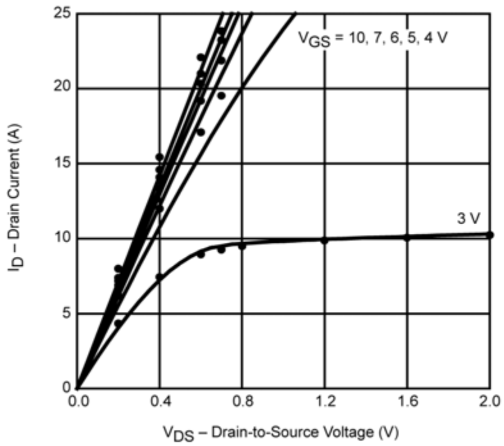
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

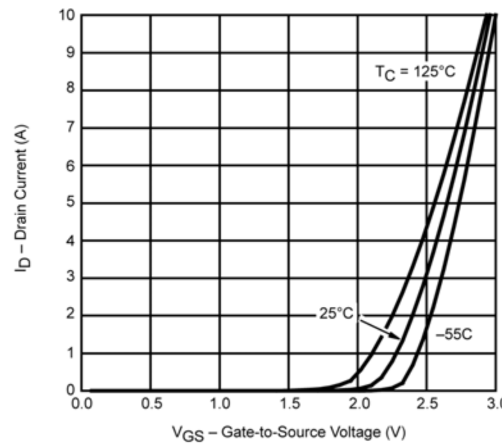
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	Ch-1	1.4		V
			Ch-2	2.1		
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, V_{GS} = 10 V	Ch-1	168		A
			Ch-2	219		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 6.5 A	Ch-1	0.028	0.027	Ω
		V_{GS} = 10 V, I_D = 7.4 A	Ch-2	0.021	0.022	
		V_{GS} = 4.5 V, I_D = 5.9 A	Ch-1	0.031	0.032	
		V_{GS} = 4.5 V, I_D = 6.6 A	Ch-2	0.024	0.029	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 6.5 A	Ch-1	16	22	S
		V_{DS} = 15 V, I_D = 7.4 A	Ch-2	17	21	
Diode Forward Voltage[a]	V_{SD}	I_S = 5.2 A	Ch-1	0.85	0.80	V
		I_S = 5.9 A	Ch-2	0.85	0.80	
Dynamic[b]						
Input Capacitance	C_{iss}	Channel 1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Channel 2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	580	570	pF
			Ch-2	662	720	
Input Capacitance	C_{oss}		Ch-1	84	80	
			Ch-2	98	115	
Reverse Transfer Capacitance	C_{rss}		Ch-1	35	35	
			Ch-2	51	50	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 6.5 A	Ch-1	12	9.5	nC
		V_{DS} = 15 V, V_{GS} = 10 V, I_D = 7.4 A	Ch-2	10	12	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 6.5 A Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 7.4 A	Ch-1	4.5	4.5	
			Ch-2	5.2	5.5	
Gate-Source Charge	Q_{gs}		Ch-1	1.5	1.5	
			Ch-2	2.5	2.5	
Gate-Drain Charge	Q_{gd}		Ch-1	1.2	1.2	
			Ch-2	1.7	1.7	

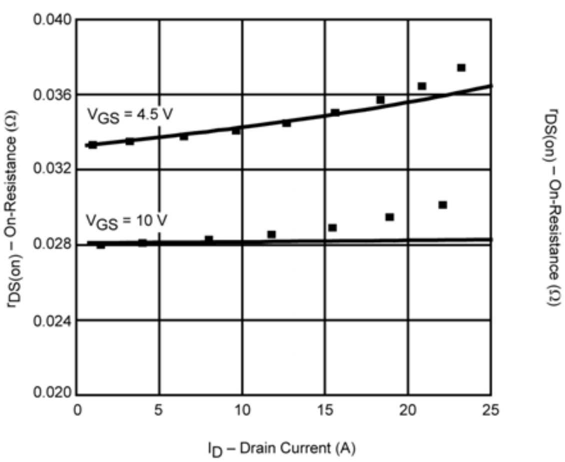
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

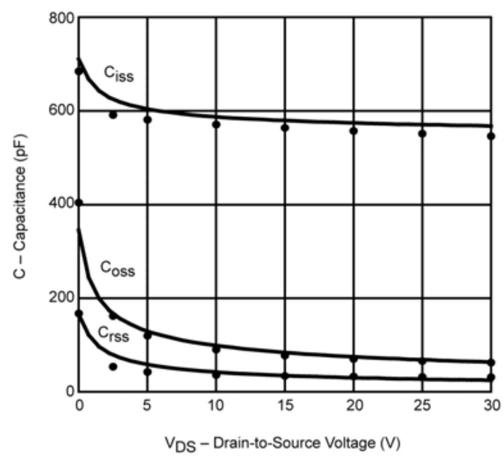
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

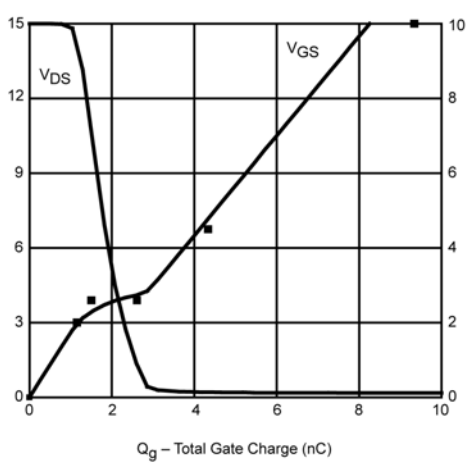
Channel 1

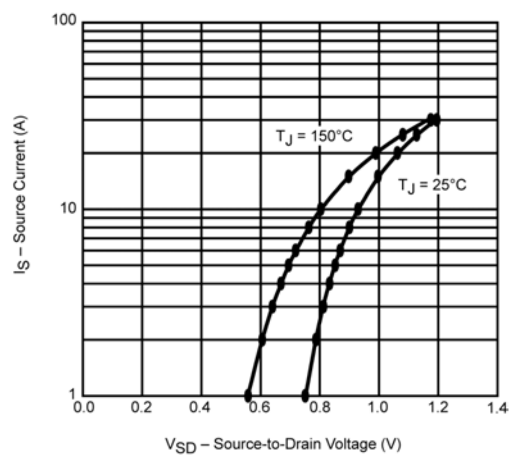






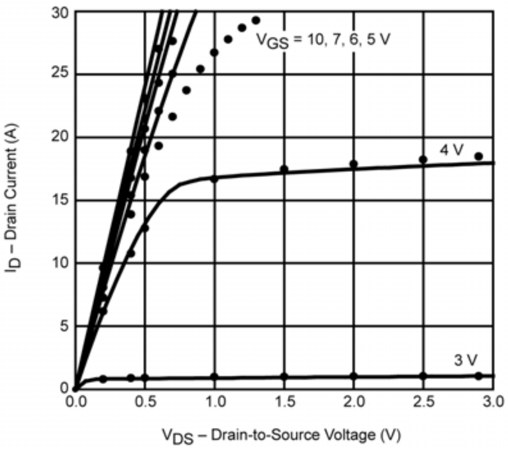


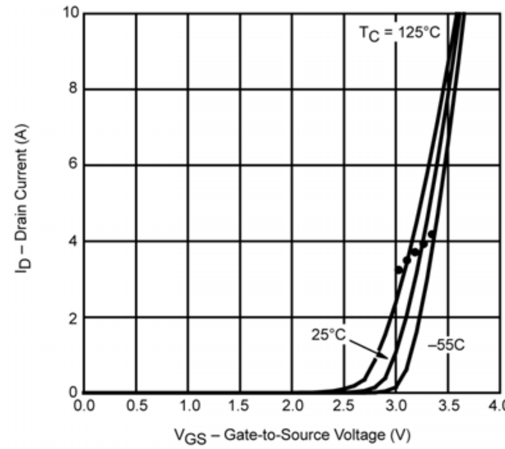


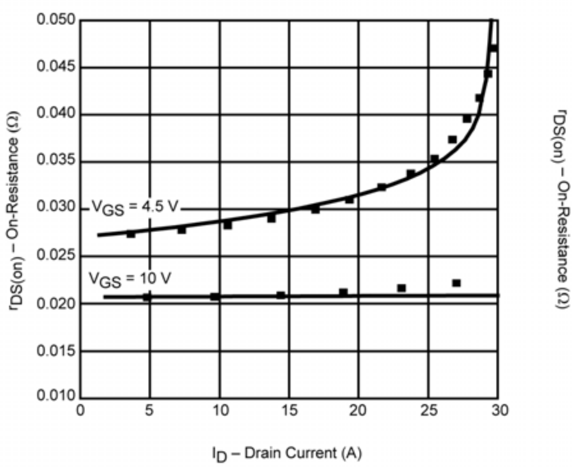


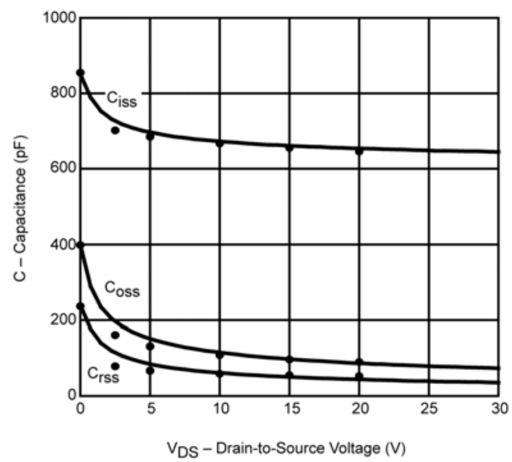
Note: Dots and squares represent measured data.

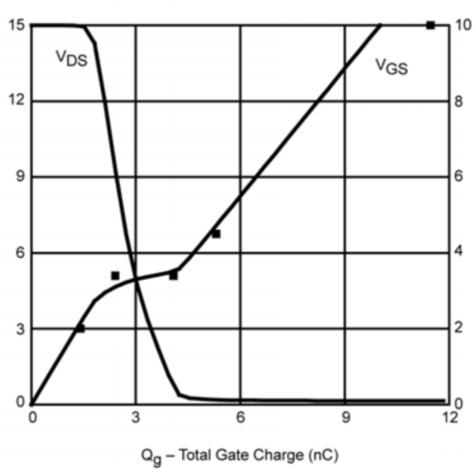
Channel 2

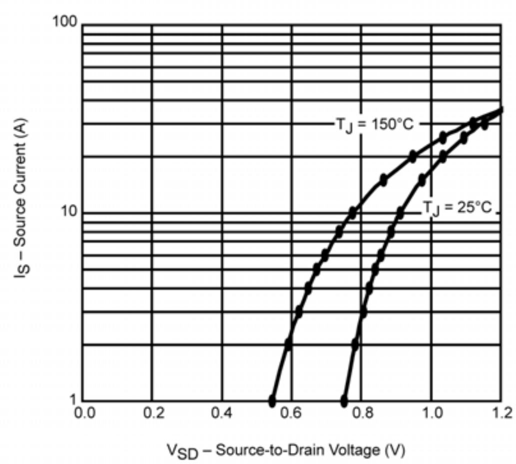












Note: Dots and squares represent measured data.

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